REMARKS

Please reconsider the application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering this application.

I. Disposition of Claims

Claims 1-11 are pending in this application. By way of this reply, claims 1, 2, 4-6, and 11 have been amended.

II. Claim Amendments

Claim 1 has been amended to refer to a method for reducing signed load latency in transfer of data from a cache memory to another element in a microprocessor comprising transferring data from the cache memory to an aligner. No new matter has been added by way of this amendment as support for this amendment may be found, for example, paragraph [0005] of the present application.

Claim 2 has been amended to recite selecting the sign bit during transfer to the aligner via the bypass. No new matter has been added by way of this amendment as support for this amendment may be found, for example, in Figure 5 of the present application.

Claim 4 has been amended to recite processing the part of the data selected for use in generating the sign bit based on an instruction from a CPU. No new matter has been added by way of this amendment as support for this amendment may be found, for example, in Figure 5 of the present application.

Claim 5 has been amended to recite an apparatus for reducing signed load latency in transfer of data from a cache memory to another element in a microprocessor comprising a data path connecting the cache memory to an aligner. No new matter has been added by way of this amendment as support for this amendment may be found, for example, in paragraph [0005] of the present application.

Claim 6 has been amended to recite a select component for providing signals to choose the sign bit for the data. No new matter has been added by way of this amendment as support for this amendment may be found, for example, in Figure 5 of the present application.

Claim 11 has been amended to recite a select component for providing signals to choose the sign bit for the data. No new matter has been added by way of this amendment as support for this amendment may be found, for example, in Figure 5 of the present application.

III. Rejection(s) under 35 U.S.C § 112

Claims 1-11 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. For the reasons set forth below, withdrawal of the rejection is respectfully requested.

Claims 1 and 5

Independent claims 1 and 5 were rejected as being unclear as to (1) from where to where the data is loaded for the latency to be measured and how the latency is reduced, (2) the difference between the data path and bypass and why a sign bit is transferred via a

bypass when the sign bit is transferred along with the data to the aligner, and (3) the function of the aligner.

With respect to (1) and (3), the data is loaded from the cache memory to another element in the microprocessor. Specification, paragraph [0005]. The aligner arranges the data from the different memory banks in the appropriate order and, if necessary, may assign a unique extension for data bits according to the CPU instructions, before transferring the data to another element in the microprocessor. Specification, paragraph [0005]. The aligner would be instructed to assign a unique extension to the data if the bit data is converted to another type. Specification, paragraph [0008]. This process is known as signing data bits. Specification, paragraph [0008].

The latency of the data transfer is determined by the time of the signing process as the aligner's signing process consumes the most time during the data transfer. Specification, paragraph [0009]. The present invention reduces the latency of the data transfer by generating the sign bit for the data while the data is being transferred to the aligner, providing the aligner with this sign bit, and hence, eliminating the aligner's signing process from the data transfer process. *See* Specification, paragraph [0010]. Hence, claims 1 and 5 have been amended to recite reducing signed load latency in transfer of data from a cache memory to another element in a microprocessor. Thus, with respect to (1) and (3), amended claims 1 and 5 are now clear and not indefinite.

With respect to (2), Figure 5 of the present application shows the data path and a bypass **50**. The data bits from the SRAM **32** are transferred along the data path to the aligner **38**. The data bits are selectively arranged and transferred through the bypass **50** to obtain the candidate bits. Candidate bits are a group of bits that include the sign bit for

the data transferred to the aligner **38** along the data path. Specification, paragraph [0025]. Through a selective processing of data as instructed by the CPU **12**, the sign bit for the data transferred to the aligner is selected by the bypass **50** and is supplied to the aligner **38** at the same time the data arrives at the aligner **38**. As a result, the latency originating from signing data bits in the aligner is eliminated, reducing the cache memory latency and increasing the performance of the microprocessor. Hence, by transferring the sign bit to the aligner through the bypass **50**, the signed load latency in the microprocessor is reduced. Thus, with respect to (2), amended claims 1 and 5 are now clear and not indefinite. Accordingly, withdrawal of the § 112 rejection of claims 1 and 5 is respectfully requested.

Claim 2

Claim 2 was rejected as being unclear as to what is performed by "adjusting." Figure 6 of the present application shows an example of arrangement of data and candidate bit sets during transfer from the SRAM **32** to another element in the microprocessor. The SRAM **32** may include a number of memory banks. In this example, the SRAM **32** consists of 4 memory banks, with each memory bank outputting 64 bits of data. The Stretcher **140** adjusts the data by shrinking or extending it for timing purposes. The data is then passed on to the MUX **34** which will once again adjust the data, by selecting 64 bits of data from one of the memory banks in accordance with the CPU **12** instructions.

The candidate bits, which include the sing bit, are passed through the bypass **50**. As the candidate bits make their way through the bypass **50**, to the aligner **38**, the sign bit is selected by the Sign MUX **52** and Real-Sign MUX **54** in accordance with the CPU **12**

instructions. Thus, claim 2 has been amended to recite selecting the sign bit during transfer to the aligner via the bypass. Accordingly, amended claim 2 is now clear and not indefinite, and the withdrawal of the § 112 rejection of claim 2 is respectfully requested.

Claims 3 and 4

Claims 3 and 4 were rejected for being unclear as to what is performed by "selectively processing" a part of the data. The candidate bits are delivered to the bypass **50** which will select one of the candidate bits as the signed bit. *See* Specification, paragraphs [0025], [0026], and [0027]. As shown in Figures 7 and 8 of the present application, in one or more embodiments of the present invention, the candidate bits are *selected* from the most significant bits of the bytes of data. Specification, paragraph [0031].

Once this part of the data is *selected*, it is then *processed* through the Sign MUX **52** and the Real-sign MUX **54** to generate the sign bit. *See* Specification, paragraph [0033]. The generation of the sign bit by the Sign MUX **52** and the Real-sign MUX **54** is controlled by the instructions **36, 90** provided by the CPU **12**. Specification, paragraphs [0026] and [0027]. Thus, the most significant bits of the bytes of data are *selected* and then *processed* through the bypass **50** in accordance with CPU **12** instructions to obtain the sign bit that is delivered to the aligner **38**. Hence, claim 4 has been amended to recite processing a part of the data selected for use in generating the sign bit based on an instruction from a CPU. Thus, with respect to what is performed by selective processing of a part of the data, claims 3 and 4 are now clear and not indefinite. Accordingly, withdrawal of the § 112 rejections of claims 3 and 4 is respectfully requested.

Claim 6

Claim 6 of the present application was rejected because it was deemed that "select component providing a signal to generate a sing bit" is inconsistent with "transfer of the sign bit from the cache memory."

As discussed above and shown in Figures 7 and 8 of the present application, the candidate bits are selected from the data output of the SRAM **32**, with each SRAM **32** memory bank providing one candidate byte (8 bits). *See* Specification, paragraph [0032]. These candidate bytes are then passed through the bypass **50**. Specification, paragraph [0033]. The candidate bytes from the various memory banks of the SRAM **50** are first passed through the Sign MUX **52**. Specification, paragraph [0033]. The select component provides the Sign MUX **52** with a signal **90** in accordance with the CPU **12** instructions. Specification, paragraph [0026]. Depending on the signal generated **90** by the select component **56**, the Sign MUX **52** will select the candidate byte from one of the memory banks. Specification, paragraph [0033].

This selected candidate byte is then passed to the Real-sign MUX **54**. Specification, paragraph [0033]. The select component will then generate a signal **36** to the Real-sign MUX **54** in accordance with the CPU **12** instructions. *See* Specification, paragraph [0027]. Based on the signal received **36** the Real-sign MUX **54** will then select one bit from the 8 candidate bits it received from the Sign MUX **54**. Specification, paragraph [0027]. This selected bit is the sign bit that is then passed on to the Aligner **38** and used to create a signed load. Specification, paragraph [0027]. Hence, the sign bit, along with the other candidate bits, is *transferred* from the cache memory to the bypass

50. Specification, paragraph [0025]. The sign bit is then chosen from amongst the candidate bits depending on the select signals provided by the select component **56**. *See* Specification, paragraphs [0031], [0032], and [0033]. The sign bit is then *transferred* to the aligner. Specification, paragraph [0033]. Accordingly, claim 6 has been amended to recite a select component for providing signals to choose the sign bit for the data. Thus, claim 6 of the present application is now clear and is not indefinite since "select component providing signals to choose a sign bit" is consistent with "transfer of the sign bit from the cache memory." Accordingly, withdrawal of the § 112 rejection of claim 6 is respectfully requested.

Claims 7 and 11

Claims 7 and 11 of the present application were rejected for being unclear as to the difference between the sign multiplexer and the real sign multiplexer. As shown in Figure 5 of the present application, the candidate bytes from the various memory banks of the SRAM **32** enter the bypass **50** and are first passed through the Sign MUX **52**. Specification, paragraph [0026]. The Sign MUX **52** uses the select signal **90** generated in response to the CPU instructions to choose *one candidate byte* from one of the memory banks. Specification, paragraph [0033].

The selected candidate *byte* is then passed on to the Real-sign MUX **54**. Specification, paragraph [0033]. The Real-sign MUX **54** will then select *one bit* from the *candidate byte*, using the select signal **36** generated in response to the CPU instructions to make this choice. Specification, paragraph [0027]. This selected bit is the sign bit that is then transferred to the aligner **38**. Specification, paragraph [0033]. Hence, Sign MUX **52** is responsible for selecting one byte, out of all the candidate bytes, and the Real-sign

MUX **54** is responsible for selecting one bit from the candidate byte selected by the Sign MUX **52**. Thus, claims 7 and 11 of the present application are clear and are not indefinite because the difference between the Sign MUX **52** and the Real-sign MUX **54** are clear to one skilled in the art. Accordingly, withdrawal of the § 112 rejections of claims 7 and 11 is respectfully requested.

Claim 10

Independent claim 10 was rejected for being unclear as to (1) the difference between the data path and bypass and why a sign bit is transferred via a bypass when a sign bit is transferred along with the data to the aligner, and (2) what is performed by selective processing. With respect to (1), the difference between the data path and the bypass and the reason for the sign bit to be transferred via a by pass are addressed in the above discussion regarding the § 112 rejection of claim 1 of the present application. With respect to (2), the meaning of selective processing is discussed above and clarified in response to § 112 rejections of claims 3 and 4 of the present application. Hence, for the reasons stated above, claim 10 of the present application is clear and is not indefinite. Accordingly, withdrawal of the § 112 rejection of claim 10 is respectfully requested.

Claim 11

Independent claim 11 was rejected as being unclear as to (1) the difference between the data path and bypass and why a sign bit is transferred via a bypass when a sign bit is transferred along with the data to the aligner, (2) the function of the aligner, and (3) consistency of "select component providing a signal bit to generate a sign bit" and the "transfer of the sign bit from the cache memory." With respect to (1), the difference between the data path and the bypass and the reason for the sign bit to be transferred via a

by pass are addressed in the above discussion regarding the § 112 rejection of claim 1 of the present application.

With respect to (2), the function of the aligner is discussed above and clarified in response to the rejection of claim 1 on the same ground. With respect to (3), claim 11 has been amended to recite a select component for providing signals to choose the sign bit for the data. As discussed above, in the response to the § 112 rejection of claim 6 of the present application, the amendment to claim 11, similar to the amendment to claim 6, makes this claim consistent because "select component providing signals to choose a sign bit" is consistent with "transfer of the sign bit from the cache memory." Thus, claim 11 is now clear and is not indefinite. Accordingly, withdrawal of the § 112 rejection of claim 11 is respectfully requested.

In view of the above, amended independent claims 1,5, 10, and 11 and dependent claims 2-7 are not indefinite, and accordingly, withdrawal of the § 112 rejections of these claims is respectfully requested. Other dependent claims are likewise not indefinite.

IV. Rejection(s) under 35 U.S.C § 102

Claims 1-11 of the present application were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,638,312 issued to Simone (hereinafter "Simone"). For the reasons set forth below, this rejection is respectfully traversed.

One of the limits to increasing the frequency of a microprocessor is the speed of data transfer from the microprocessor's cache memory to other elements in the microprocessor. As shown in Figure 3 of the present application, in a typical system, the data from the SRAM **32** is first transferred to the Stretcher ("STR") **140** that extends or

shrinks signal of the data to adjust the timing during data transfer. After the timing is adjusted, the data is transferred to a multiplexer (MUX) **34** that may select a part of the data using the signal **36** from the CPU **12**. The chosen data is then transferred to an aligner **38**, which arranges the data in appropriate order and, if necessary, may assign a unique extension for data bits according to the instructions. The aligner **38** will then transfer the data **40** to an other element in the microprocessor. The latency of the above system is generally determined by the signing process in the aligner as this process consumes the most time during the data transfer.

The present invention is directed to improving the speed of data transfer from a cache memory to one or more other elements in the microprocessor by eliminating the time elapsed in the aligner **38** to sign the data. Specification, paragraph [0023]-[0024]. With reference to the exemplary embodiment of the present invention shown in Figure 5 of the present application, the sign bit is selected in a bypass **50** at the same time the data is being transferred to the aligner **38**. Specification, paragraph [0024]. The candidate bytes are first selected and passed into the bypass **50**. *See* Specification, paragraphs [0032] and [0033]. The Sign MUX **52** will then choose one of the candidate bytes depending on the select signal **90** generated in accordance with the CPU **12** instructions. Specification, paragraph [0033].

The candidate byte selected, which consists of 8 candidate bits, is then transferred to the Real-sign MUX **54**. Specification, paragraph [0033]. The Real-sign MUX **54** will use the select signal **36** from the CPU **12** instructions to choose one bit from the candidate byte as the sign bit. Specification, paragraph, [0027]. This sign bit is then

transferred to the aligner **38** with the data and hence, the aligner need not consume any time to come up with the sign bit. *See* Specification, paragraph [0011].

Accordingly, amended independent claim 1 of the present application requires, in part, *transferring the sign bit to the aligner via a bypass*. Amended independent claim 5 of the present application requires, in part, *a bypass connecting the cache memory to the aligner,* wherein *a sign bit for the data is transferred from the cache memory to the aligner via the bypass*. Independent claim 10 of the present application requires, in part, *means for transferring the sign bit to the aligner via a bypass*. Amended independent claim 11 of the present application requires, in part, *a bypass connecting the cache memory to the aligner*, wherein *a sign bit for the data is transferred from the cache memory to the aligner along the bypass*.

Simone, in contrast to the present application, fails to disclose at least the limitations of independent claims 1, 5, 10, and 11 discussed above. Simone discloses a method and apparatus for generating a zero flag (z-flag) status signal in a microprocessor for unaligned data, simultaneous to the load alignment of such data. *See* Simone, Abstract. As shown in Figure 2 of Simone, the bypass circuit in Simone *does not* connect the cache memory **101** to the load aligner **102**. Instead, the bypass circuit in Simone bypasses the load aligner **102** and is connected to the control circuit. Thus, the output from the bypass circuit is *not transferred to the aligner* and *does not effect the time elapsed in the aligner for the signing process*. As such, Simone fails to disclose or otherwise teach, any improvements to data transfer by reducing the time consumed in the load aligner in generating the sign bit.

Accordingly, Simone fails to disclose, or otherwise teach, improving the speed of data transfer from the cache memory to other elements in the microprocessor using the bypass to generate the sign bit and eliminating the consumption of time in the aligner to generate this bit as required by independent claims 1, 5, 10, and 11 of the present application. In view of the above, Simone fails to show or suggest the present invention as recited in independent claims 1, 5, 10, and 11. Thus, independent claims 1, 5, 10, and 11 of the present application are patentable over Simone. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

V. Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places the present application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.035001).

Respectfully submitted,

Date: 8/27/04

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